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| APPLICATION NO. | FILING DATE | FIRST NAMED INVENTOR | ATTORNEY DOCKET NO. | CONFIRMATION NO. |
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| 10/099,801 | 03/13/2002 | Ching-Song Yang | JCLA8216 | 3084 |

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| EXAMINER | |
|---|---|
| WARREN, MATTHEW E | |

| ART UNIT | PAPER NUMBER |
|---|---|
| 2815 | |

DATE MAILED: 12/17/2003

Please find below and/or attached an Office communication concerning this application or proceeding.

| Office Action Summary | Application No. 10/099,801 | Applicant(s) YANG ET AL. | |
|---|---|---|---|
| | Examiner Matthew E. Warren | Art Unit 2815 | A.W |

*-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --*

**Period for Reply**

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

**Status**

1)☒ Responsive to communication(s) filed on *13 March 2002*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

**Disposition of Claims**

4)☒ Claim(s) *1-11* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-7 and 9-11* is/are rejected.

7)☒ Claim(s) *8* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

**Application Papers**

9)☒ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

**Priority under 35 U.S.C. §§ 119 and 120**

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

13)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application) since a specific reference was included in the first sentence of the specification or in an Application Data Sheet. 37 CFR 1.78.

a) ☐ The translation of the foreign language provisional application has been received.

14)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121 since a specific reference was included in the first sentence of the specification or in an Application Data Sheet. 37 CFR 1.78.

**Attachment(s)**

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449) Paper No(s) _____.
4) ☐ Interview Summary (PTO-413) Paper No(s). _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other:

## DETAILED ACTION

### *Specification*

The title of the invention is not descriptive. A new title is required that is clearly indicative of the invention to which the claims are directed.

### *Claim Objections*

Claims 10 and 11 are objected to because of the following informalities: claims 9 and 10 each contain grammatical errors in the first and second lines of the claims. Appropriate correction is required.

### *Claim Rejections - 35 USC § 103*

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claims 1, 2, and 4-7 are rejected under 35 U.S.C. 103(a) as being unpatentable over Nishimoto et al. (US 6,444,514 B1) in view of Abedifard (US Pub. 2002/0074592 A1).

In re claim 1, Nishimoto et al. shows (figs. 4 and 5) a non-volatile semiconductor memory cell comprising a substrate (1) having a shallow first type (p-type) well layer (4),

a second-type (n-type) well layer (3) and a deep first type (p) well layer (2), wherein the deep first type well layer is at a greater depth than the shallow first type well layer. The second type well layer is between the shallow first type well layer and the deep first-type well layer. A plurality of stacked gates (M) are formed above the shallow first type well layer of the substrate. A plurality of source (9) and drain (10) terminals are formed between the stack gates. The source and drain terminals are second type (n) doped regions since the channel between the source and drain has a first type doping due to the first type doping of the well layer (4). Nishimoto shows all of the elements of the claims except the depth of the source terminal is long enough to pass through the shallow first type well layer and connect with the second type well layer. Abedifard shows (fig. 2B) a memory cell having a source terminal (206 and 210) which is long enough to pass through the shallow first type (p-type) well layer (204) and connect with the second type (n-type) well layer (202). The source is terminal and drain (208) are second type (n) doped regions. With this configuration, the source-line resistance is improved without the need for metal lines, thus permitting a greater packing density of memory cells (paragraph [0060]. Therefore it would have been obvious to one of ordinary skill in the art at the time the invention was made to modify the source terminal of Nishimoto by extending the source terminal through a shallow well layer as taught by Abedifard to improve the source-line resistance and ultimately increase the packing density.

In re claim 2, Nishimoto discloses (col. 10, lines 7-13) that a various well layers have the desired doping and also shows that the source and drain terminals are second

type (n) doped regions since the channel between the source and drain has a first type doping due to the first type doping of the well layer (4).

In re claim 4, Nishimoto shows (figs. 4 and 5) that a first dielectric (6) is over the substrate, a floating gate (7, 8) is over the first dielectric, a second dielectric layer (9) is over the floating gate, and a control gate (12, 13) is over the dielectric layer.

In re claim 5, Nishimoto discloses (col. 11, lines 40-42) that the second dielectric (9) includes an oxide/nitride/oxide composite layer.

In re claims 6 and 7, Nishimoto discloses (col. 11, lines 30-42) that a first dielectric (oxide portion of composite layer 9) is over the substrate, a trap layer (nitride portion of composite layer 9) is over the first dielectric, a second dielectric layer (oxide portion of composite layer 9) is over the trap layer, and a control gate (12, 13) is over the second dielectric layer.

Claims 3, and 9-11 are rejected under 35 U.S.C. 103(a) as being unpatentable over Nishimoto et al. (US 6,444,514 B1) in view of Abedifard (US Pub. 2002/0074592 A1) as applied to claim 1 above, and further in view of Hsu et al. (US Pub. 2002/0185673 A1).

In re claim 3, Nishimoto et al. in view of Abedifard shows all of the elements of the claims except the shallow well, the deep well, second type well, and the source and drain having the desired type of doping. Nishimoto had already disclosed one type of doping scheme (consistent with claim 2) however did not mention the situation in which the dopant types were reverse. It is well known in the art the transistor regions having

on type of doping can be switched with the other type of doping. However, Hsu et al. discloses that the P-type and N-type semiconductor regions of the memory device can be interchanged with each other (paragraph [0029]). Therefore it would have been obvious to one of ordinary skill in the art at the time the invention was made to modify the doped regions of Nishimoto and Abedifard by interchanging the doping types because Hsu teaches that such well known substitutions will form the opposite type of semiconductor device.

In re claims 9-11, Nishimoto in view of Abedifard show all of the elements of the claims except the limitations concerning the drain terminal and shallow terminal being shorted. Hsu et al. shows (fig. 3) a memory cell structure in which a drain (25) and a shallow first type (p) well layer (27) are shorted. A metal contact (39) is located across an exposed surface of the drain terminal and penetrates through a junction between the drain terminal and the shallow first type well layer. With this configuration, the programming operation will have reduced disturbances (paragraph [0008]). Therefore it would have been obvious to one of ordinary skill in the art at the time the invention was made to modify the drain of Nishimoto and Abedifard by shorting the drain with a shallow region as taught by Hsu to reduce errors during the memory programming operation.

### *Allowable Subject Matter*

Claim 8 is objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

### *Conclusion*

The prior art made of record and not relied upon is considered pertinent to applicant's disclosure. Suwa et al. (JP 05-006971 A) also discloses a memory device having various well regions.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Matthew E. Warren whose telephone number is (703) 305-0760. The examiner can normally be reached on Mon-Thurs, and alternating Fri, 9:00-5:00.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Tom Thomas can be reached on (703) 308-2772. The fax phone number for the organization where this application or proceeding is assigned is (703) 305-3432.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is (703) 308-0956.

Matthew E. Warren
December 13, 2003